MVC100
Hardware Introduction

MicroVision Co., Ltd.

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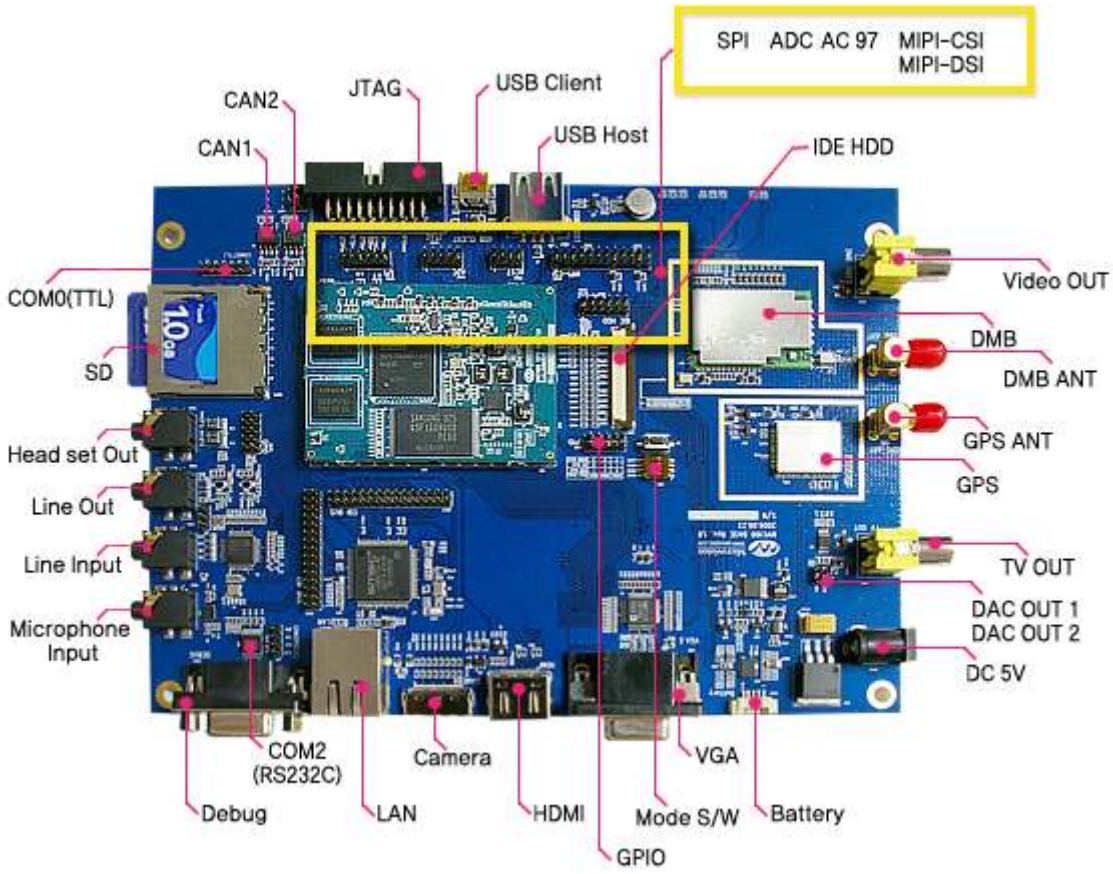
1. MVC100 Introduction

This solution board is based on Samsung S5PC100 (667/800MHz) Cortex-A8 32Bit RISC Processor. It supports Built-in HD level image (1280/1024), Multi- Format Video Codec MPEG-4, H.264/H.263, MPEG-2, WMV9, Divx, Xvid and Out-put TV out for NTSC/PAL, Digital TV HDMI on CPU and it can support other USB OTG 2.0, CAN Interface, OpenGL 3D. Also it is possible to boot USB and SD Card. This board is full solution board which developers can have all specification test (Full Spec.) like High Function Mobile Device (PMP, DMB, NAVI), Industry Control / System Control Device as it consumes lower power and is more efficient than previous ARM board.

- Equipped with S5PC100 (667/800MHz) based on Samsung Cortex A8 Core
- Equipped with High function, Low-Cost memory device for mass production
- Google Android OS Porting
- 7" Wide TFT-LCD to development the luxury navigation
- Equipped with DMB Module for hand carry and watch the broadcasting
- Equipped with Bluetooth module
- Equipped with high-resolution Camera Module for hand carry DVR and movie filming, screen capture
- Realization of high speed USB 2.0 for optimum development environment
- Support various Boot Mode
- Realization of HDD Interface for hand carries devices
- Equipped with battery only for mobile and realization of charge circuit for mass production mobile device

2. MVC100 Specification

MAIN BOARD

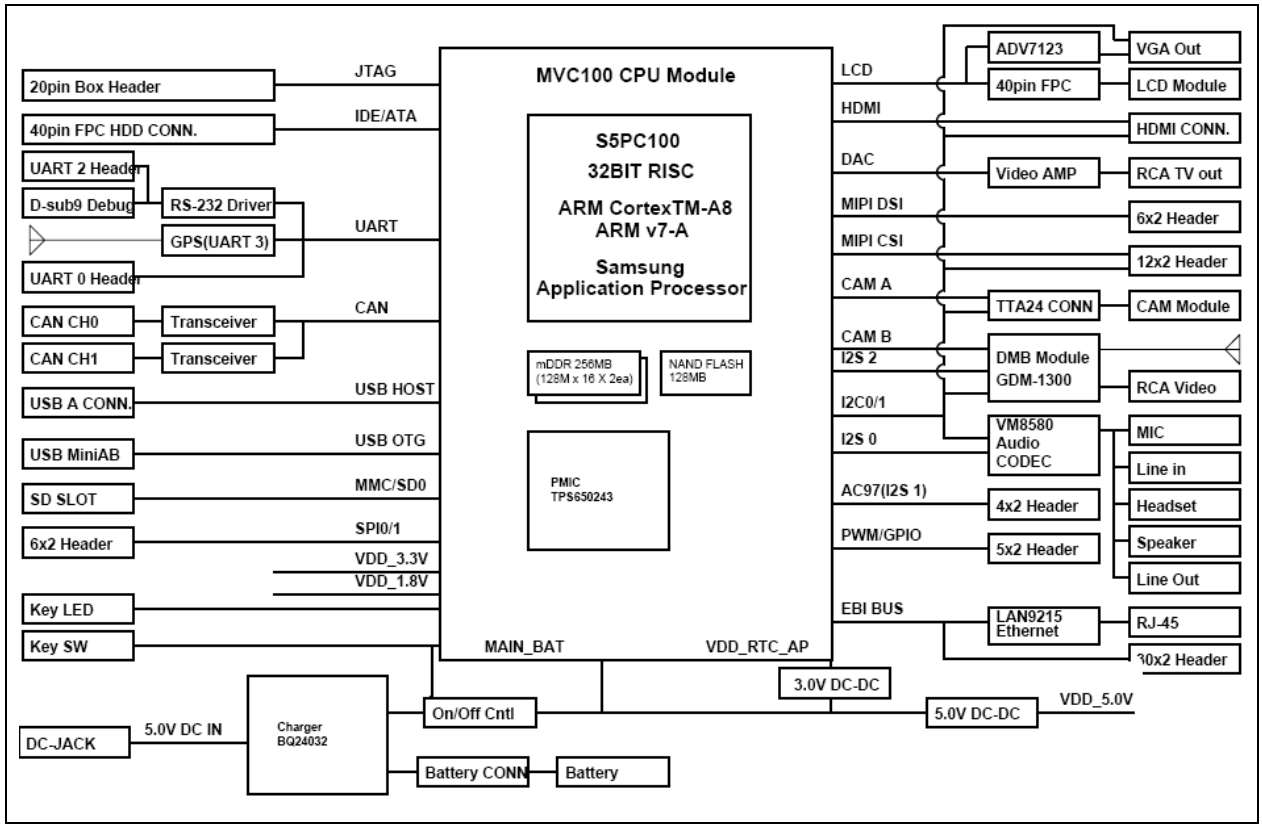


BASE BOARD

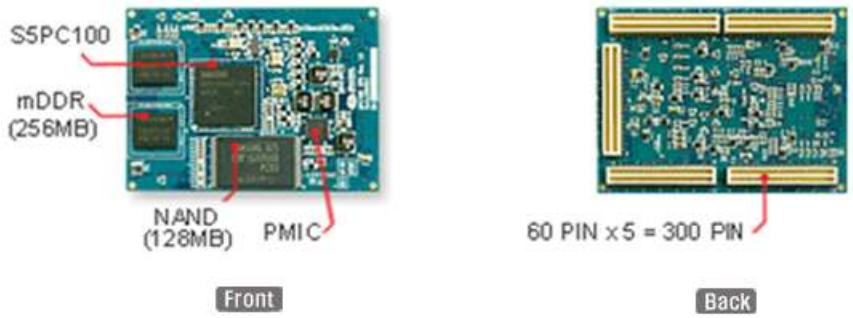
3. H/W Specification

ITEM	SPEC&PART	DESCRIPTION
CPU	S5PC100	Cortex A8 Core, 667/800MHz
RAM	Samsung mDDR	256MByte, 32Bit Access, Clock Speed 266MHz
NAND Flash	Samsung NAND	Large Block 2GB(256MByte)
NOR Flash	AMD	NOR Flash 8MB (1MByte), 16Bit (Limit 64KBit)
Audio Codec	I2S	I2S 5.1Ch, Lower Power MP3 Play Mode, WM8580, Stereo 400mW Output Speaker, MIC IN, Head SET, AC97Header
Graphic	2D/3D	Support 2D/3D Graphic Controller
USB	2Ports	USB Host 1.1 , USB OTG 2.0(Not provide BSP)
MIPI	2Ports	MIPI-CSI(Camera) 1Port, MIPI-DSI(LCD) 1Port
CAN	2Ch	Ver2.0, 1Mbps, Transceiver built-in(Not provide BSP)
Video(TV-Out)	1Port	NTSC/PAL Composite
HDMI	1Port	1.2 HDMI Standard 19Pin Connector (576P, 720P Resolution)
LCD	7" LCD	7" WVGA LCD / 800X480
VGA(1280*1024)	1Port	Analog VGA 1280*1024 up to 2048*2048 (VGA D-SUB 15PIN)
DMB	GDM1300	Built-In H/W Codec, NTSC / PAL Composite Out-put
GPS	Gaon GPS	SiRF Star III, GPS Engine Module
Camera	Aptina 2M Pixel	Support Auto Focus , Preview & Snap Shot function
Ethernet	SMSC9215	Support 10/100Base-T, Link/ACT/Speed LED
SD Slot	1Port	SD Host & SD Memory V2.0 Compliant
HDD(Option)	1Port	Provide FPC/FFC Connector Interface (Not provide BSP)
Wi-Fi(Option)	USB Type	Wi-Fi 802.11g, Support WPA/WPA2 , Provide USB Interface
Battery (Option)	1530mAH @3.7V	Full Operation more than 1 Hour , Provide Battery Interface
Charger, PMIC	BQ24032	AC & Battery Switching function, Battery Connector
Others	Ports	SPI, I2C, UART 3Ports, EBI, JTAG, Key 4EA, LED 2EA

4. MVC100 Block Diagram



6. Main Board Pins



- Parts posting and compact size for mass production
- Miniaturize (60X44) CPU Module
- Support various extension functions with providing Extension connector
- Possible to reuse the main CPU Module by modification of Base Board when manufacture the mass production

Pad	Name	Function Signals				Pull	I/O	PDN	VDD	MVC100
XuRXD[0]	GPA0[0]	UART0_RXD				PD	I	A1	VDDQ_EXT	JP3(TTL level) EXT UART RXD
XuTXD[0]	GPA0[1]	UART0_TXD				PD	I	A1	VDDQ_EXT	JP3(TTL level) EXT UART TXD
XuCTSn[0]	GPA0[2]	UART0_CTSn				PD	I	A1	VDDQ_EXT	JP3(TTL level) EXT UART CTSn
XuRTSn[0]	GPA0[3]	UART0_RTSn				PD	I	A1	VDDQ_EXT	JP3(TTL level) EXT UART RTSn
XuRXD[1]	GPA0[4]	UART1_RXD				PD	I	A1	VDDQ_EXT	Debug UART RxD
XuTXD[1]	GPA0[5]	UART1_TXD				PD	I	A1	VDDQ_EXT	Debug UART TxD
XuCTSn[1]	GPA0[6]	UART1_CTSn				PD	I	A1	VDDQ_EXT	Power on lock output, High=lock enable
XuRTSn[1]	GPA0[7]	UART1_RTSn				PD	I	A1	VDDQ_EXT	Line output jack plug in detect, Low = jack insert
XuRXD[2]	GPA1[0]	UART2_RXD				PD	I	A1	VDDQ_EXT	AUX, JP2 RS-232 4pin header
XuTXD[2]	GPA1[1]	UART2_TXD				PD	I	A1	VDDQ_EXT	AUX, JP2 RS-232 4pin header
XuRXD[3]	GPA1[2]	UART3_RXD	UART2_CTSn	IrDA_RXD		PD	I	A1	VDDQ_EXT	GPS UART RXD
XuTXD[3]	GPA1[3]	UART3_TXD	UART2_RTSn	IrDA_TXD		PD	I	A1	VDDQ_EXT	GPS UART TXD
XuCLK	GPA1[4]	UARTCLK	IrDA_SDBW			PD	I	A1	VDDQ_EXT	Line input jack plug in detect, Low = jack insert
XspiMISO[0]	GPB[0]	SPIO_MISO				PD	I	A1	VDDQ_EXT	SPIO EXT(CN35)
XspiCLK[0]	GPB[1]	SPIO_CLK				PD	I	A1	VDDQ_EXT	SPIO EXT(CN35)

XspiMOSI[0]	GPB[2]	SPIO_MOSI				PD	I	A1	VDDQ_EXT	SPIO EXT(CN35)
XspiCSn[0]	GPB[3]	SPIO_nCS				PD	I	A1	VDDQ_EXT	SPIO EXT(CN35)
XspiMISO[1]	GPB[4]	SPI1_MISO				PD	I	A1	VDDQ_EXT	SPI1 EXT(CN35)
XspiCLK[1]	GPB[5]	SPI1_CLK				PD	I	A1	VDDQ_EXT	SPI1 EXT(CN35)
XspiMOSI[1]	GPB[6]	SPI1_MOSI				PD	I	A1	VDDQ_EXT	SPI1 EXT(CN35)
XspiCSn[1]	GPB[7]	SPI1_nCS				PD	I	A1	VDDQ_EXT	SPI1 EXT(CN35)
XI2S1SCLK	GPC[0]	I2S1_SCLK	PCM1_SCLK	AC97_BITCLK		PD	I	A1	VDDQ_AUD	AC97 EXT(CN34)
XI2S1CDCLK	GPC[1]	I2S1_CDCLK	PCM1_EXTCLK	AC97_RESETn		PD	I	A1	VDDQ_AUD	AC97 EXT(CN34)
XI2S1LRCK	GPC[2]	I2S1_LRCK	PCM1_FSYNC	AC97_SYNC		PD	I	A1	VDDQ_AUD	AC97 EXT(CN34)
XI2S1SDI	GPC[3]	I2S1_SDI	PCM1_SIN	AC97_SDI		PD	I	A1	VDDQ_AUD	AC97 EXT(CN34)
XI2S1SDO	GPC[4]	I2S1_SDO	PCM1_SOUT	AC97_SDO		PD	I	A1	VDDQ_A	AC97 EXT(CN34)
XpwmTOUT[0]	GPD[0]	TOUT0	PWM_TCLK			PD	I	A1	VDDQ_EXT	LCD Backlight dimming control PWM
XpwmTOUT[1]	GPD[1]	TOUT1	EX_DMA_REQn			PD	I	A1	VDDQ_EXT	GPIO EXT(CN39)
XpwmTOUT[2]	GPD[2]	TOUT2	EX_DMA_ACKn			PD	I	A1	VDDQ_EXT	GPIO EXT(CN39)
XI2C0SDA	GPD[3]	I2C0_SDA				PD	I	A1	VDDQ_EXT	I2C data WM8580/DMB/CAM
XI2C0SCL	GPD[4]	I2C0_SCL				PD	I	A1	VDDQ_EXT	I2C Clock WM8580/DMB/CAM
XI2C1SDA	GPD[5]	I2C1_SDA	SPDIF_0_OUT			PD	I	A1	VDDQ_EXT	I2C data HDMI/VGA SMB bus serial data
XI2C1SCL	GPD[6]	I2C1_SCL	SPDIF_EXTCLK			PD	I	A1	VDDQ_EXT	I2C Clock HDMI/VGA SMB bus serial clock
XciPCLK	GPE0[0]	CAM_A_PCLK	SD1_CLK			PD	I	A1	VDDQ_CI	CAM I/F CAM_A_PCLK
XciVSYNC	GPE0[1]	CAM_A_VSYNC	SD1_CDn			PD	I	A1	VDDQ_CI	CAM I/F CAM_A_VSYNC
XciHREF	GPE0[2]	CAM_A_HREF	SD1_CMD			PD	I	A1	VDDQ_CI	CAM I/F CAM_A_HREF
XciD[0]	GPE0[3]	CAM_A_D[0]	SD1_D[0]			PD	I	A1	VDDQ_CI	CAM I/F CAM_A_D[0]
XciD[1]	GPE0[4]	CAM_A_D[1]	SD1_D[1]			PD	I	A1	VDDQ_CI	CAM I/F CAM_A_D[1]
XciD[2]	GPE0[5]	CAM_A_D[2]	SD1_D[2]			PD	I	A1	VDDQ_CI	CAM I/F CAM_A_D[2]
XciD[3]	GPE0[6]	CAM_A_D[3]	SD1_D[3]			PD	I	A1	VDDQ_CI	CAM I/F CAM_A_D[3]
XciD[4]	GPE0[7]	CAM_A_D[4]	SD1_D[4]			PD	I	A1	VDDQ_CI	CAM I/F CAM_A_D[4]
XciD[5]	GPE1[0]	CAM_A_D[5]	SD1_D[5]			PD	I	A1	VDDQ_CI	CAM I/F CAM_A_D[5]
XciD[6]	GPE1[1]	CAM_A_D[6]	SD1_D[6]			PD	I	A1	VDDQ_CI	CAM I/F CAM_A_D[6]
XciD[7]	GPE1[2]	CAM_A_D[7]	SD1_D[7]			PD	I	A1	VDDQ_CI	CAM I/F CAM_A_D[7]
XciCLKenb	GPE1[3]	CAM_A_CLKOUT				PD	I	A1	VDDQ_CI	CAM I/F CAM_A_CLKOUT
XciRESET	GPE1[4]	CAM_A_RESET				PD	I	A1	VDDQ_CI	CAM I/F CAM_A_RESET

XciFIELD	GPE1[5]	CAM_A_FIELD				PD	I	A1	VDDQ_CI	GPIO (CN42)
XvHSYNC	GPF0[0]	LCD_HSYNC	SYS_CS0	VEN_HSYNC		PD	I	A1	VDDQ_LCD	LCD I/F
XvVSYNC	GPF0[1]	LCD_VSYNC	SYS_CS1	VEN_VSYNC		PD	I	A1	VDDQ_LCD	LCD I/F
XvVDEN	GPF0[2]	LCD_VDEN	SYS_RS	VEN_HREF		PD	I	A1	VDDQ_LCD	LCD I/F
XvVCLK	GPF0[3]	LCD_VCLK	SYS_WE	V601_CLK		PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[0]	GPF0[4]	LCD_VD[0]	SYS_VD[0]	VEN_D[0]		PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[1]	GPF0[5]	LCD_VD[1]	SYS_VD[1]	VEN_D[1]		PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[2]	GPF0[6]	LCD_VD[2]	SYS_VD[2]	VEN_D[2]		PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[3]	GPF0[7]	LCD_VD[3]	SYS_VD[3]	VEN_D[3]		PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[4]	GPF1[0]	LCD_VD[4]	SYS_VD[4]	VEN_D[4]		PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[5]	GPF1[2]	LCD_VD[5]	SYS_VD[5]	VEN_D[5]		PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[6]	GPF1[2]	LCD_VD[6]	SYS_VD[6]	VEN_D[6]		PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[7]	GPF1[3]	LCD_VD[7]	SYS_VD[7]	VEN_D[7]		PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[8]	GPF1[4]	LCD_VD[8]	SYS_VD[8]	V656_D[0]		PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[9]	GPF1[5]	LCD_VD[9]	SYS_VD[9]	V656_D[1]		PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[10]	GPF1[6]	LCD_VD[10]	SYS_VD[10]	V656_D[2]		PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[11]	GPF1[7]	LCD_VD[11]	SYS_VD[11]	V656_D[3]		PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[12]	GPF2[0]	LCD_VD[12]	SYS_VD[12]	V656_D[4]		PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[13]	GPF2[1]	LCD_VD[13]	SYS_VD[13]	V656_D[5]		PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[14]	GPF2[2]	LCD_VD[14]	SYS_VD[14]	V656_D[6]		PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[15]	GPF2[3]	LCD_VD[15]	SYS_VD[15]	V656_D[7]		PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[16]	GPF2[4]	LCD_VD[16]	SYS_VD[16]			PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[17]	GPF2[5]	LCD_VD[17]	SYS_VD[17]			PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[18]	GPF2[6]	LCD_VD[18]				PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[19]	GPF2[7]	LCD_VD[19]				PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[20]	GPF3[0]	LCD_VD[20]				PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[21]	GPF3[1]	LCD_VD[21]				PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[22]	GPF3[2]	LCD_VD[22]	VSYNC_LDI	V656_CLK		PD	I	A1	VDDQ_LCD	LCD I/F
XvVD[23]	GPF3[3]	LCD_VD[23]	SYS_OE	VEN_FIELD		PD	I	A1	VDDQ_LCD	LCD I/F
XmmcOCLK	GPG0[0]	SD0_CLK				PD	I	A1	VDDQ_EXT	SD I/F SD0_CLK
XmmcOCMD	GPG0[1]	SD0_CMD				PD	I	A1	VDDQ_EXT	SD I/F SD0_CMD
XmmcOD[0]	GPG0[2]	SD0_D[0]				PD	I	A1	VDDQ_EXT	SD I/F SD0_D[0]
XmmcOD[1]	GPG0[3]	SD0_D[1]				PD	I	A1	VDDQ_EXT	SD I/F SD0_D[1]
XmmcOD[2]	GPG0[4]	SD0_D[2]				PD	I	A1	VDDQ_EXT	SD I/F SD0_D[2]

XmmcOD[3]	GPGO[5]	SDO_D[3]				PD	I	Al	VDDQ_EXT	SD I/F SDO_D[3]
XmmcOD[4]	GPGO[6]	SDO_D[4]				PD	I	Al	VDDQ_EXT	LED2 LOW = LED2 ON
XmmcOD[5]	GPGO[7]	SDO_D[5]				PD	I	Al	VDDQ_EXT	GPS_RESET, High= normal operation (not use)
XmmcOD[6]	GPGl[0]	SDO_D[6]				PD	I	Al	VDDQ_EXT	LAN9215 reset, High = normal operation
XmmcOD[7]	GPGl[1]	SDO_D[7]				PD	I	Al	VDDQ_EXT	DMB_nRESET, High=normal operation
XmmcOCDn	GPGl[2]	SDO_CDn				PD	I	Al	VDDQ_EXT	SD I/F SDO_CDn, Low = Card inserted
XmmclCLK	GPG2[0]	SDl_CLK				PD	I	Al	VDDQ_EXT	Speaker AMP enable, High= enable
XmmclCMD	GPG2[1]	SDl_CMD				PD	I	Al	VDDQ_EXT	LCD_5.0V_EN, High = power on
XmmclD[0]	GPG2[2]	SDl_D[0]				PD	I	Al	VDDQ_EXT	LCD_3.3V_EN, High = power on
XmmclD[1]	GPG2[3]	SDl_D[1]				PD	I	Al	VDDQ_EXT	VGA_EN, Low = VGA power save mode, High=normal
XmmclD[2]	GPG2[4]	SDl_D[2]				PD	I	Al	VDDQ_EXT	GPS power enable(3.3V) High=enable
XmmclD[3]	GPG2[5]	SDl_D[3]				PD	I	Al	VDDQ_EXT	DMB power enable(3.3V/1.8B/1.2V) High=enable
XmmclCDn	GPG2[6]	SDl_CDn				PD	I	Al	VDDQ_EXT	USB HOST Power enable, High=power enable
Xmmc2CLK	GPG3[0]	SD2_CLK	SPI2_CLK	I2S2_SCLK	PCMO_SCLK	PD	I	Al	VDDQ_MMC	DMB DAC_BCLK
Xmmc2CMD	GPG3[1]	SD2_CMD	SPI2_nSS	I2S2_CDCLK	PCMO_EXTCLK	PD	I	Al	VDDQ_MMC	DMB DAC_MCLK
Xmmc2DATA[0]	GPG3[2]	SD2_D[0]	SPI2_MISO	I2S2_LRCK	PCMO_FSYNC	PD	I	Al	VDDQ_MMC	DMB DAC_LRCK
Xmmc2DATA[1]	GPG3[3]	SD2_D[1]	SPI2_MOSI	I2S2_SDI	PCMO_SIN	PD	I	Al	VDDQ_MMC	DMB DAC_CATA
Xmmc2DATA[2]	GPG3[4]	SD2_D[2]	I2S2_SDO	PCMO_SOUT		PD	I	Al	VDDQ_MMC	Switch S5 input High active
Xmmc2DATA[3]	GPG3[5]	SD2_D[3]	SPDIF_OUT			PD	I	Al	VDDQ_MMC	Switch S4 input High active
Xmmc2CDn	GPG3[6]	SD2_CDn	SPDIF_EXTCLK			PD	I	Al	VDDQ_MMC	Switch S3 input High active
XEINT[0]	GPHO[0]	WKUP_INT[0]				PD	I	B	VDDQ_SYSO	Not use
XEINT[1]	GPHO[1]	WKUP_INT[1]				PD	I	B	VDDQ_SYSO	Not use
XEINT[2]	GPHO[2]	WKUP_INT[2]				PD	I	B	VDDQ_SYSO	Not use
XEINT[3]	GPHO[3]	WKUP_INT[3]				PD	I	B	VDDQ_SYSO	Not use

XEINT[4]	GPH0[4]	WKUP_INT[4]				PD	I	B	VDDQ_SYS0	Not use
XEINT[5]	GPH0[5]	WKUP_INT[5]				PD	I	B	VDDQ_SYS0	Not use
XEINT[6]	GPH0[6]	WKUP_INT[6]				PD	I	B	VDDQ_SYS0	Not use
XEINT[7]	GPH0[7]	WKUP_INT[7]				PD	I	B	VDDQ_SYS0	Not use
XEINT[8]	GPH1[0]	WKUP_INT[8]				PD	I	B	VDDQ_SYS5	Not use
XEINT[9]	GPH1[1]	WKUP_INT[9]				PD	I	B	VDDQ_SYS5	GPIO(CN42)
XEINT[10]	GPH1[2]	WKUP_INT[10]	CG_REALIN			PD	I	B	VDDQ_SYS5	LAN9215 interrupt. Low = interrupt occurred
XEINT[11]	GPH1[3]	WKUP_INT[11]	CG_IMGIN			PD	I	B	VDDQ_SYS5	DMB Interrupt input. Low = interrupt occurred
XEINT[12]	GPH1[4]	WKUP_INT[12]	CG_GPO[0]			PD	I	B	VDDQ_SYS5	USB HOST Current Fault Low = fault occurred
XEINT[13]	GPH1[5]	WKUP_INT[13]	CG_GPO[1]			PD	I	B	VDDQ_SYS5	HDMI_DETECT interrupt. LOW= HDMI present
XEINT[14]	GPH1[6]	WKUP_INT[14]	CG_GPO[2]			PD	I	B	VDDQ_SYS5	CAM Auto Focus done
XEINT[15]	GPH1[7]	WKUP_INT[15]	CG_GPO[3]			PD	I	B	VDDQ_SYS5	USB OTG Current Fault Low = fault occurred
XEINT[16]	GPH2[0]	WKUP_INT[16]	KP_COL[0]	CAM_B_D[0]		PD	I	B	VDDQ_SYS0	DMB CAM DATA0
XEINT[17]	GPH2[1]	WKUP_INT[17]	KP_COL[1]	CAM_B_D[1]		PD	I	B	VDDQ_SYS0	DMB CAM DATA1
XEINT[18]	GPH2[2]	WKUP_INT[18]	KP_COL[2]	CAM_B_D[2]		PD	I	B	VDDQ_SYS0	DMB CAM DATA2
XEINT[19]	GPH2[3]	WKUP_INT[19]	KP_COL[3]	CAM_B_D[3]		PD	I	B	VDDQ_SYS0	DMB CAM DATA3
XEINT[20]	GPH2[4]	WKUP_INT[20]	KP_COL[4]	CAM_B_D[4]		PD	I	B	VDDQ_SYS0	DMB CAM DATA4
XEINT[21]	GPH2[5]	WKUP_INT[21]	KP_COL[5]	CAM_B_D[5]		PD	I	B	VDDQ_SYS0	DMB CAM DATA5
XEINT[22]	GPH2[6]	WKUP_INT[22]	KP_COL[6]	CAM_B_D[6]		PD	I	B	VDDQ_SYS0	DMB CAM DATA6
XEINT[23]	GPH2[7]	WKUP_INT[23]	KP_COL[7]	CAM_B_D[7]		PD	I	B	VDDQ_SYS0	DMB CAM DATA7
XEINT[24]	GPH3[0]	WKUP_INT[24]	KP_ROW[0]	CAM_B_PCLK		PD	I	B	VDDQ_SYS0	DMB CAM_PCLK
XEINT[25]	GPH3[1]	WKUP_INT[25]	KP_ROW[1]	CAM_B_VSYNC		PD	I	B	VDDQ_SYS0	Headset plug in detect. Low = jack insert
XEINT[26]	GPH3[2]	WKUP_INT[26]	KP_ROW[2]	CAM_B_HREF		PD	I	B	VDDQ_SYS0	Power switch. Low= power key pressed
XEINT[27]	GPH3[3]	WKUP_INT[27]	KP_ROW[3]	CAM_B_FIELD		PD	I	B	VDDQ_SYS0	Switch S6 input High active. wake-up interrupt
XEINT[28]	GPH3[4]	WKUP_INT[28]	KP_ROW[4]	CAN0_TX		PD	I	B	VDDQ_CAN	CAN0 TX
XEINT[29]	GPH3[5]	WKUP_INT[29]	KP_ROW[5]	CAN0_RX		PD	I	B	VDDQ_CAN	CAN0 RX

XEINT[30]	GPH3[6]	WKUP_INT[30]	KP_ROW[6]	CAN1_TX		PD	I	B	VDDQ_CAN	CAN1 TX
XEINT[31]	GPH3[7]	WKUP_INT[31]	KP_ROW[7]	CAN1_RX		PD	I	B	VDDQ_CAN	CAN1 RX
XiemSCLK	GPI[0]	IEM_SCLK				PD	I	A1	VDDQ_MMC	MIC Pre. AMP enable, Low=shutdown
XiemSPWI	GPI[1]	IEM_SPWI				PD	I	A1	VDDQ_MMC	MIC plug in detect, High = jack insert
XNFMOD[0]	GPI[2]	NFMOD[0]				-	I	C	VDDQ_SYSO	boot mode SW1-3
XNFMOD[1]	GPI[3]	NFMOD[1]				-	I	C	VDDQ_SYSO	boot mode (Fix to 1)
XNFMOD[2]	GPI[4]	NFMOD[2]				PD	I	A1	VDDQ_SYS2	boot mode (Fix to 0)
XNFMOD[3]	GPI[5]	NFMOD[3]				PD	I	A1	VDDQ_SYS2	boot mode (Fix to 1)
XNFMOD[4]	GPI[6]	NFMOD[4]				PD	I	A1	VDDQ_SYS2	boot mode (Fix to 1)
XNFMOD[5]	GPI[7]	NFMOD[5]				PD	I	A1	VDDQ_SYS2	boot mode SW1-2
XmsmADDR[0]	GPJ0[0]	MSM_A[0]	HSI_TXD	CF_A[0]		PD	I	A1	VDDQ_MSM	HDD I/F
XmsmADDR[1]	GPJ0[1]	MSM_A[1]	HSI_TX_FLAG	CF_A[1]		PD	I	A1	VDDQ_MSM	HDD I/F
XmsmADDR[2]	GPJ0[2]	MSM_A[2]	HSI_TX_WAKE	CF_A[2]		PD	I	A1	VDDQ_MSM	HDD I/F
XmsmADDR[3]	GPJ0[3]	MSM_A[3]	HSI_TX_READY	CF_IORDY		PD	I	A1	VDDQ_MSM	HDD I/F IDE_RDY
XmsmADDR[4]	GPJ0[4]	MSM_A[4]	HSI_RXD	CF_INTRQ		PD	I	A1	VDDQ_MSM	HDD I/F
XmsmADDR[5]	GPJ0[5]	MSM_A[5]	HSI_RX_FLAG	CF_INPACKn		PD	I	A1	VDDQ_MSM	HDD I/F
XmsmADDR[6]	GPJ0[6]	MSM_A[6]	HSI_RX_WAKE	CF_RESET		PD	I	A1	VDDQ_MSM	HDD I/F
XmsmADDR[7]	GPJ0[7]	MSM_A[7]	HSI_RX_READY	CF_REG		PD	I	A1	VDDQ_MSM	HDD I/F
XmsmADDR[8]	GPJ1[0]	MSM_A[8]				PD	I	A1	VDDQ_MSM	GPIO EXT(CN39)
XmsmADDR[9]	GPJ1[1]	MSM_A[9]				PD	I	A1	VDDQ_MSM	GPIO EXT(CN39)
XmsmADDR[10]	GPJ1[2]	MSM_A[10]				PD	I	A1	VDDQ_MSM	GPIO EXT(CN39)
XmsmADDR[11]	GPJ1[3]	MSM_A[11]				PD	I	A1	VDDQ_MSM	GPIO EXT(CN39)
XmsmADDR[12]	GPJ1[4]	MSM_A[12]				PD	I	A1	VDDQ_MSM	GPIO EXT(CN39)
XmsmDATA[0]	GPJ2[0]	MSM_D[0]	CF_D[0]			PD	I	A1	VDDQ_MSM	HDD I/F
XmsmDATA[1]	GPJ2[1]	MSM_D[1]	CF_D[1]			PD	I	A1	VDDQ_MSM	HDD I/F
XmsmDATA[2]	GPJ2[2]	MSM_D[2]	CF_D[2]			PD	I	A1	VDDQ_MSM	HDD I/F
XmsmDATA[3]	GPJ2[3]	MSM_D[3]	CF_D[3]			PD	I	A1	VDDQ_MSM	HDD I/F
XmsmDATA[4]	GPJ2[4]	MSM_D[4]	CF_D[4]			PD	I	A1	VDDQ_MSM	HDD I/F
XmsmDATA[5]	GPJ2[5]	MSM_D[5]	CF_D[5]			PD	I	A1	VDDQ_MSM	HDD I/F
XmsmDATA[6]	GPJ2[6]	MSM_D[6]	CF_D[6]			PD	I	A1	VDDQ_MSM	HDD I/F
XmsmDATA[7]	GPJ2[7]	MSM_D[7]	CF_D[7]			PD	I	A1	VDDQ_MSM	HDD I/F
XmsmDATA[8]	GPJ3[0]	MSM_D[8]	CF_D[8]			PD	I	A1	VDDQ_MSM	HDD I/F

XmsmDATA[9]	GPJ3[1]	MSM_D[9]	CF_D[9]			PD	I	A1	VDDQ_MSM	HDD I/F
XmsmDATA[10]	GPJ3[2]	MSM_D[10]	F_D[10]			PD	I	A1	VDDQ_MSM	HDD I/F
XmsmDATA[11]	GPJ3[3]	MSM_D[11]	F_D[11]			PD	I	A1	VDDQ_MSM	HDD I/F
XmsmDATA[12]	GPJ3[4]	MSM_D[12]	CF_D[12]			PD	I	A1	VDDQ_MSM	HDD I/F
XmsmDATA[13]	GPJ3[5]	MSM_D[13]	CF_D[13]			PD	I	A1	VDDQ_MSM	HDD I/F
XmsmDATA[14]	GPJ3[6]	MSM_D[14]	CF_D[14]			PD	I	A1	VDDQ_MSM	HDD I/F
XmsmDATA[15]	GPJ3[7]	MSM_D[15]	CF_D[15]			PD	I	A1	VDDQ_MSM	HDD I/F
XmsmCSn	GPJ4[0]	MSM_CSn	CF_nCS[0]			PD	I	A1	VDDQ_MSM	HDD I/F
XmsmWEn	GPJ4[1]	MSM_WEn	CF_nCS[1]			PD	I	A1	VDDQ_MSM	HDD I/F
XmsmRn	GPJ4[2]	MSM_REn	CF_IORDn			PD	I	A1	VDDQ_MSM	HDD I/F
XmsmIRQn	GPJ4[3]	MSM_IRQn	CF_IOWRn			PD	I	A1	VDDQ_MSM	HDD I/F
XmOCSn[0]	GPK0[0]	SMC_nCS[0]				-	OH	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOCSn[1]	GPK0[1]	SMC_nCS[1]				-	OH	A2	VDDQ_MO	LAN9215 chip select
XmOCSn[2]	GPK0[2]	SMC_nCS[2]	NF_nCS[0]	OND_nCS[0]		-	OH	A2	VDDQ_MO	NAND chip select(boot device)
XmOCSn[3]	GPK0[3]	SMC_nCS[3]	NF_nCS[1]	OND_nCS[1]		-	OH	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOCSn[4]	GPK0[4]	SMC_nCS[4]	NF_nCS[2]	CF_nCS[0]		-	OH	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOCSn[5]	GPK0[5]	SMC_nCS[5]	NF_nCS[3]	CF_nCS[1]		-	OH	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOOEn	GPK0[6]	EBI_OEn				-	OH	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOWEn	GPK0[7]	EBI_WEn				-	OH	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOBEn[0]	GPK1[0]	EBI_BEn[0]				-	OH	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOBEn[1]	GPK1[1]	EBI_BEn[1]				-	OH	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOWAITn	GPK1[2]	SMC_WAITn				PU	I	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmODATA_RDn	GPK1[3]	EBI_DATA_RDn				-	OH	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOCFOEn	GPK1[4]	CF_OEn				-	OH	A2	VDDQ_MO	GPIO EXT(CN38)
XmOCFWEn	GPK1[5]	CF_WEn				-	OH	A2	VDDQ_MO	GPIO EXT(CN38)
XmOFCLE	GPK2[0]	NF_CLE	OND_AVALID			-	OL	A2	VDDQ_MO	NAND I/F
XmOFALE	GPK2[1]	NF_ALE	OND_SMCLK			-	OL	A2	VDDQ_MO	NAND I/F
XmOFWEn	GPK2[2]	NF_WEn	OND_RPn			-	OH	A2	VDDQ_MO	NAND I/F
XmOFREn	GPK2[3]	NF_REn				-	OH	A2	VDDQ_MO	NAND I/F
XmOFRnB[0]	GPK2[4]	NF_RnB[0]	OND_INT[0]			PD	I	A2	VDDQ_MO	NAND I/F
XmOFRnB[1]	GPK2[5]	NF_RnB[1]	OND_INT[1]			PD	I	A2	VDDQ_MO	NAND I/F
XmOFRnB[2]	GPK2[6]	NF_RnB[2]				PU	I	A2	VDDQ_MO	NAND I/F
XmOFRnB[3]	GPK2[7]	NF_RnB[3]				PU	I	A2	VDDQ_MO	NAND I/F
XmOIORDY	GPK3[0]	CF_IORDY				PD	I	A2	VDDQ_MO	5.0V supply enable.

										High=power enable
XmOINTRQ	GPK3[1]	CF_INTRQ				PD	I	A2	VDDQ_MO	DC-IN adaptor present, Low=DC-IN present
XmORESET	GPK3[2]	CF_RESET				-	OL	A2	VDDQ_MO	GPIO EXT(CN38)
XmOINPACKn	GPK3[3]	CF_INPACKn				PU	I	A2	VDDQ_MO	GPIO EXT(CN38)
XmOREG	GPK3[4]	CF_REG				-	OL	A2	VDDQ_MO	GPIO EXT(CN38)
XmOCDn	GPK3[5]	CF_CDn				PU	I	A2	VDDQ_MO	GPIO EXT(CN38)
XmOIORDn	GPK3[6]	CF_IORDn				-	OH	A2	VDDQ_MO	GPIO EXT(CN38)
XmOIOWRn	GPK3[7]	CF_IOWRn				-	OH	A2	VDDQ_MO	GPIO EXT(CN38)
XmOADDR[0]	GPL0[0]	EBI_A[1]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[1]	GPL0[1]	EBI_A[1]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[2]	GPL0[2]	EBI_A[2]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[3]	GPL0[3]	EBI_A[3]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[4]	GPL0[4]	EBI_A[4]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[5]	GPL0[5]	EBI_A[5]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[6]	GPL0[6]	EBI_A[6]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[7]	GPL0[7]	EBI_A[7]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[8]	GPL1[0]	EBI_A[8]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[9]	GPL1[1]	EBI_A[9]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[10]	GPL1[2]	EBI_A[10]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[11]	GPL1[3]	EBI_A[11]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[12]	GPL1[4]	EBI_A[12]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[13]	GPL1[5]	EBI_A[13]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[14]	GPL1[6]	EBI_A[14]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[15]	GPL1[7]	EBI_A[15]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[16]	GPL2[0]	EBI_A[16]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[17]	GPL2[1]	EBI_A[17]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[18]	GPL2[2]	EBI_A[18]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[19]	GPL2[3]	EBI_A[19]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmOADDR[20]	GPL2[4]	EBI_A[20]				-	OL	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmODATA[0]	GPL2[5]	EBI_D[0]				-	I	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmODATA[1]	GPL2[6]	EBI_D[1]				-	I	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmODATA[2]	GPL2[7]	EBI_D[2]				-	I	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmODATA[3]	GPL3[0]	EBI_D[3]				-	I	A2	VDDQ_MO	EBI BUS (CN36/CN42)

XmODATA[4]	GPL3[1]	EBI_D[4]				-	I	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmODATA[5]	GPL3[2]	EBI_D[5]				-	I	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmODATA[6]	GPL3[3]	EBI_D[6]				-	I	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmODATA[7]	GPL3[4]	EBI_D[7]				-	I	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmODATA[8]	GPL3[5]	EBI_D[8]				-	I	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmODATA[9]	GPL3[6]	EBI_D[9]				-	I	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmODATA[10]	GPL3[7]	EBI_D[10]				-	I	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmODATA[11]	GPL4[0]	EBI_D[11]				-	I	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmODATA[12]	GPL4[1]	EBI_D[12]				-	I	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmODATA[13]	GPL4[2]	EBI_D[13]				-	I	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmODATA[14]	GPL4[3]	EBI_D[14]				-	I	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XmODATA[15]	GPL4[4]	EBI_D[15]				-	I	A2	VDDQ_MO	EBI BUS (CN36/CN42)
XefFSOURCE_0	efrom_fsource_0					-	I	-	VDDQ_MO	Fix to GND
XefFVGATE_0	efrom_fvgate_0					-	I	-	VDDQ_MO	Fix to VDD_INT_AP(1.2V)
XjTMS	TMS					PU	I	E1	VDDQ_EXT	JTAG I/F
XjTCK	TCK					PU	I	E1	VDDQ_EXT	JTAG I/F
XjTDO	TDO					-	OL	E1	VDDQ_EXT	JTAG I/F
XjTDI	TDI					PU	I	E1	VDDQ_EXT	JTAG I/F
XjDBGSEL	DBGSEL					PD	I	E1	VDDQ_EXT	FIX to Low
XuhDP	UHOST_DP					-	AI	-	VDD_UH	USB HOST DP
XuhDN	UHOST_DN					-	AI	-	VDD_UH	USB HOST DN
XPWRRGTON	PWRRGTON					-	OL	B	VDDQ_SYSO	
XnRESET	nRESET					-	I	B	VDDQ_SYSO	
XnWRESET	nWRESET					-	I	B	VDDQ_SYSO	Not use (pull-up add)
XnBATF	nBATF					-	I	B	VDDQ_SYSO	Battery fault input
XOM[0]	OM[0]					-	I	B	VDDQ_SYSO	boot mode (FIX to 0)
XOM[1]	OM[1]					-	I	B	VDDQ_SYSO	boot mode (FIX to 0)
XOM[2]	OM[2]					-	I	B	VDDQ_SYSO	boot mode SW1-4
XOM[3]	OM[3]					-	I	B	VDDQ_SYSO	boot mode (FIX to 0)
XOM[4]	OM[4]					-	I	B	VDDQ_SYSO	boot mode (FIX to 0)
XXTI	XTI					-	I	-	VDDQ_SYSO	system clock input
XXTO	XTO					-	OL	-	VDDQ_SYSO	system clock input
XrtcXTI	RTC_XTI					-	I	-	VDD_RTC	system clock input
XrtcXTO	RTC_XXTO					-	OL	-	VDD_RTC	system clock input

XusbXTI	USB_XTI					-	AI	-	VDDQ_SYS2	system clock input
XusbXTO	USB_XTO					-	AO	-	VDDQ_SYS2	system clock input
X27mXTI	27M_XTI					-	I	-	VDDQ_SYS2	system clock input
X27mXTO	27M_XTO					-	OL	-	VDDQ_SYS2	system clock input
XCLKOUT	CLKOUT					-	OL	E1	VDDQ_SYS2	Test only
XnRSTOUT	nRSTOUT					-	OH	-	VDDQ_SYS2	EBI BUS (CN36/CN42)
XadcAIN[9]	ADC_IN[9]					-	I	H	VDD_ADC	Touch XP
XadcAIN[8]	ADC_IN[8]					-	I	H	VDD_ADC	Touch XM
XadcAIN[7]	ADC_IN[7]					-	I	H	VDD_ADC	Touch YP
XadcAIN[6]	ADC_IN[6]					-	I	H	VDD_ADC	Touch YM
XadcAIN[5]	ADC_IN[5]					-	I	-	VDD_ADC	ADC EXT(CN37)
XadcAIN[4]	ADC_IN[4]					-	I	-	VDD_ADC	ADC EXT(CN37)
XadcAIN[3]	ADC_IN[3]					-	I	-	VDD_ADC	ADC EXT(CN37)
XadcAIN[2]	ADC_IN[2]					-	I	-	VDD_ADC	ADC EXT(CN37)
XadcAIN[1]	ADC_IN[1]					-	I	-	VDD_ADC	ADC EXT(CN37)
XadcAIN[0]	ADC_IN[0]					-	I	-	VDD_ADC	ADC EXT(CN37)
XadcVref	ADC_VREF					-	I	-	VDD_ADC	
XusbDRVVBUS	USB_DRVVBUS					-	OL	-	VDDQ_USB	USB OTG 5.0V enable High= enable
XusbDM	USB_DM					-	AI	-	VDDQ_USB	USB OTG DM
XusbREXT	USB_REXT					-	AI	-	VDDQ_USB	External resister(Fixed)
XusbDP	USB_DP					-	AI	-	VDDQ_USB	USB OTG DP
XusbVBUS	USB_VBUS					-	AI	-	VDDQ_USB	USB OTG 5.0V input dectect
XusbID	USB_ID					-	AI	-	VDDQ_USB	USB OTG ID input
XmipiDP[5]	MIPI_DP[5]					-	I	-	VDD_MIPI	Not use (test only)
XmipiDN[5]	MIPI_DN[5]					-	I	-	VDD_MIPI	Not use (test only)
XmipiDP[4]	MIPI_DP[4]					-	I	-	VDD_MIPI	MIPI-CSI EXT(CN33)
XmipiDN[4]	MIPI_DN[4]					-	I	-	VDD_MIPI	MIPI-CSI EXT(CN33)
XmipiRXCP	MIPI_RXCP					-	OH	-	VDD_MIPI	MIPI-CSI EXT(CN33)
XmipiRXCN	MIPI_RXCN					-	OH	-	VDD_MIPI	MIPI-CSI EXT(CN33)
XmipiDP[3]	MIPI_DP[3]					-	I	-	VDD_MIPI	MIPI-CSI EXT(CN33)
XmipiDN[3]	MIPI_DN[3]					-	I	-	VDD_MIPI	MIPI-CSI EXT(CN33)
XmipiDP[2]	MIPI_DP[2]					-	OH	-	VDD_MIPI	MIPI-DSI EXT(CN32)
XmipiDPN[2]	MIPI_DN[2]					-	OH	-	VDD_MIPI	MIPI-DSI EXT(CN32)

XmipiDP[1]	MIPI_DP[1]					-	OH	-	VDD_MIPI	MIPI-DSI EXT(CN32)
XmipiDN[1]	MIPI_DN[1]					-	OH	-	VDD_MIPI	MIPI-DSI EXT(CN32)
XmipiReg_cap	MIPI_Reg_cap					-	I	-	VDD_MIPI	
XmipiTXCP	MIPI_TXCP					-	OH	-	VDD_MIPI	MIPI-DSI EXT(CN32)
XmipiTXCN	MIPI_TXCN					-	OH	-	VDD_MIPI	MIPI-DSI EXT(CN32)
XmipiDP[0]	MIPI_DP[0]					-	OH	-	VDD_MIPI	MIPI-DSI EXT(CN32)
XmipiDN[0]	MIPI_DN[0]					-	OH	-	VDD_MIPI	MIPI-DSI EXT(CN32)
XhdmiREXT	HDMI_REXT					-	I	-	VDD_HDMI	HDMI external resistor
XhdmiTXCN	HDMI_TXCN					-	OH	-	VDD_HDMI	HDMI
XhdmiTXCP	HDMI_TXCP					-	OH	-	VDD_HDMI	HDMI
XhdmiTxON	HDMI_TxON					-	OH	-	VDD_HDMI	HDMI
XhdmiTXOP	HDMI_TXOP					-	OH	-	VDD_HDMI	HDMI
XhdmiTX1N	HDMI_TX1N					-	OH	-	VDD_HDMI	HDMI
XhdmiTX1P	HDMI_TX1P					-	OH	-	VDD_HDMI	HDMI
XhdmiTX2N	HDMI_TX2N					-	OH	-	VDD_HDMI	HDMI
XhdmiTX2P	HDMI_TX2P					-	OH	-	VDD_HDMI	HDMI
XyyTCLK	CG_CLK					-	I	-	VDDQ_SYS5	I think not provide. LED1 LOW = LED1 ON, GPIO mode
XdacOUT[1]	DAC_OUT[1]					-	OH	-	VDDQ_MSM	DAC_OUT 1 AUX, CN10
XdacOUT[2]	DAC_OUT[2]					-	OH	-	VDDQ_MSM	DAC_OUT 2 AUX, CN11
XdacIREF	DAC_IREF					-	I	-	VDDQ_MSM	
XdacVREF	DAC_VREF					-	I	-	VDDQ_MSM	
XdacCOMP	DAC_COMP					-	OH	-	VDDQ_MSM	
XdacOUT[0]	DAC_OUT[0]					-	OH	-	VDDQ_MSM	DAC_OUT 0 Composit TV OUT
XI2SOLRCK	I2S0_LRCK					-	OL	E1	VDDQ_AUD	WM8580 I2S Codec
XI2SOCDCLK	I2S0_CDCLK					-	OL	E1	VDDQ_AUD	WM8580 I2S Codec
XI2SOSCLK	I2S0_SCLK					-	OL	E1	VDDQ_AUD	WM8580 I2S Codec
XI2SOSDI	I2S0_SDI					PD	I	E1	VDDQ_AUD	WM8580 I2S Codec
XI2SOSDO[0]	I2S0_SDO[0]					-	OL	E1	VDDQ_AUD	WM8580 I2S Codec
XI2SOSDO[1]	I2S0_SDO[1]					-	OL	E1	VDDQ_AUD	WM8580 I2S Codec
XI2SOSDO[2]	I2S0_SDO[2]					-	OL	E1	VDDQ_AUD	WM8580 I2S Codec